Amendments to the Specification:

Please replace the paragraph at page 6, lines 25-31 with the following amended paragraph:

FIG. 3 is a plan view of the PCB 280 for the multi-chip package shown in FIG. 2. As shown in FIG. 3, a plurality of first bonding pads 282 and a plurality of second bonding pads 283 are disposed on the PCB 280. The bonding wires 250 and 260 of the second and third semiconductor chips 220 and 230 shown in FIG. 2 are connected to the first bonding pads 282. The solder balls 211 of the first semiconductor chip 210 shown in FIG. 2 are connected to the second bonding pads 283 via a solder bumps 215 ~~(not shown)~~.

Please replace the paragraph at page 7, lines 7-13 with the following amended paragraph:

The reliability test conducted after the first semiconductor chip 410 is assembled at the package level showed good results. The first semiconductor chip 410 may be a semiconductor chip such as a flash memory having relatively high defective rate. Further, it is preferable that the package type of the first semiconductor chip 410 is a Thin Quad Flat package (TQFP) or a Super Thin Small Outline Package (STSOP). Pins 411 of the first semiconductor chip 410 are electrically connected to the PCB 480 via a solder bumps 415 ~~(not shown)~~.

Please replace the paragraph at page 8, lines 9-14 with the following amended paragraph:

FIG. 5 is a plan view of the PCB 480 for the multi-chip package shown in FIG. 4. As shown in FIG. 5, a plurality of first bonding pads 482 and a plurality of second bonding pads 483 are disposed on the PCB 480. The bonding wires 450 and 460 of the second and third semiconductor chips 420 and 430 shown in FIG. 4 are connected to the first bonding pads 482. The pins 411 of the first semiconductor chip 410 shown in FIG. 4 are connected to the second bonding pads 483 via a solder bumps 415 ~~(not shown)~~.

Please replace the paragraph at page 9, lines 20-26 with the following amended paragraph:

FIG. 7 is a plan view of the PCB 680 for the multi-chip package shown in FIG. 6. As shown in FIG. 7, a plurality of first bonding pads 682 and a plurality of second bonding pads 683 are disposed on the PCB 680. The bonding wires 650 and 660 of the second and third semiconductor chips 620 and 630 shown in FIG. 6 are connected to the first bonding pads 682. The solder balls 611 of the first semiconductor chip 610 shown in FIG. 6 are connected to the second bonding pads 683 via [[a]] solder bumps 615 ~~(not shown)~~.

Please replace the paragraph at page 10, lines 3-8 with the following amended paragraph:

The reliability test conducted after the first semiconductor chip 810 is assembled at the package level showed good results. The first semiconductor chip 810 may be a semiconductor chip such as a flash memory having relatively high defective rate. Further, it is preferable that the package type of the first semiconductor chip 810 is a TQFP or a STSOP. Pins 811 of the first semiconductor chip 810 are electrically connected to the PCB 880 via [[a]] solder bumps 815 ~~(not shown)~~.

Please replace the paragraph at page 11, lines 3-8 with the following amended paragraph:

FIG. 9 is a plan view of the PCB 880 for the multi-chip package shown in FIG. 8. As shown in FIG. 9, a plurality of first bonding pads 882 and a plurality of second bonding pads 883 are disposed on the PCB 880. The bonding wires 850 and 860 of the second and third semiconductor chips 820 and 830 shown in FIG. 8 are connected to the first bonding pads 882. The pins 811 of the first semiconductor chip 810 shown in FIG. 8 are connected to the second bonding pads 883 via [[a]] solder bumps 815 ~~(not shown)~~.